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None

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(54) MRC diversity circuit uses branch with maximum RSSI

(57) A delayed detection MRC (maximum ratio composition) diversity circuit does not adjust synchronization in every reception branch independently. The circuit has a comparison circuit 5 for selecting the reception branch with maximum received signal strength, a selector 6, a base-band circuit such as a synchronization circuit 8 for generating a regenerated clock by adjusting bit synchronization in terms of the reception branch with the maximum received signal strength, and an MRC diversity circuit section 15 for actually composing an output signal using the regenerated clock.

F I G. 3

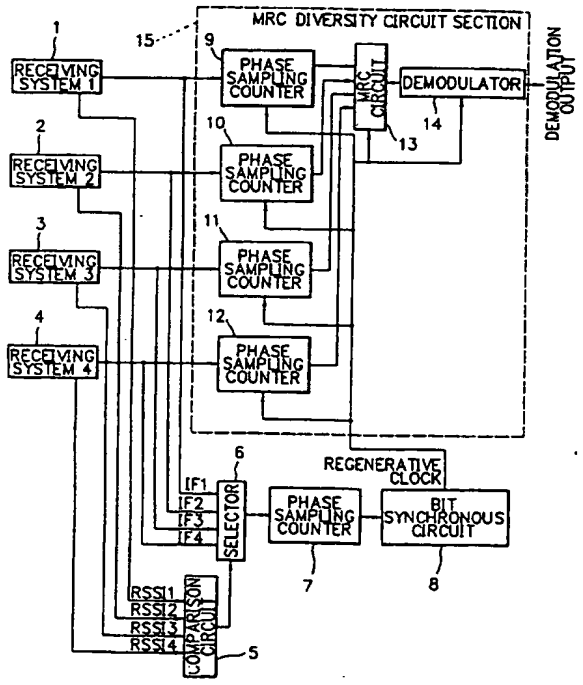

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FIG. 1 PRIOR ART

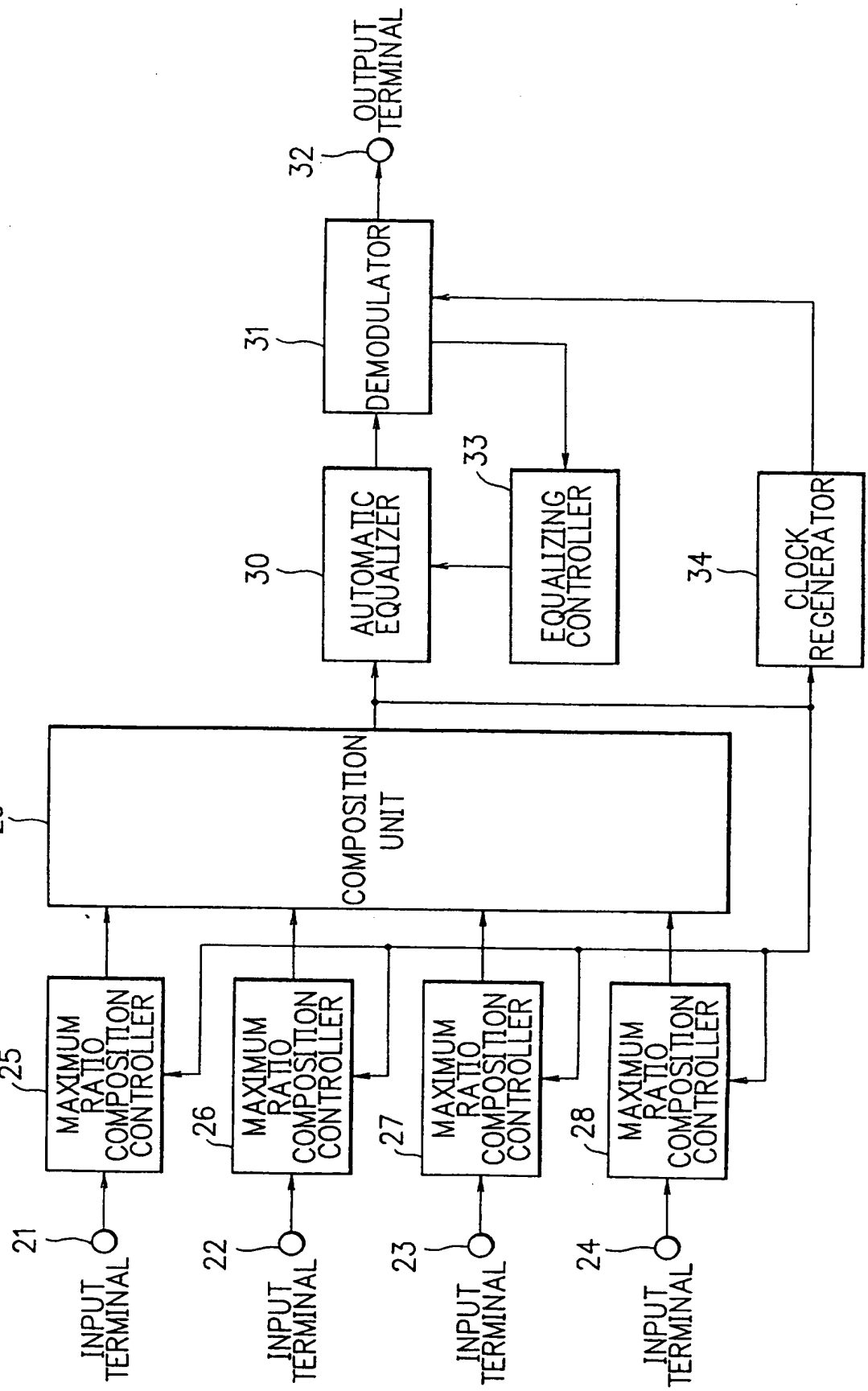


FIG. 2 PRIOR ART

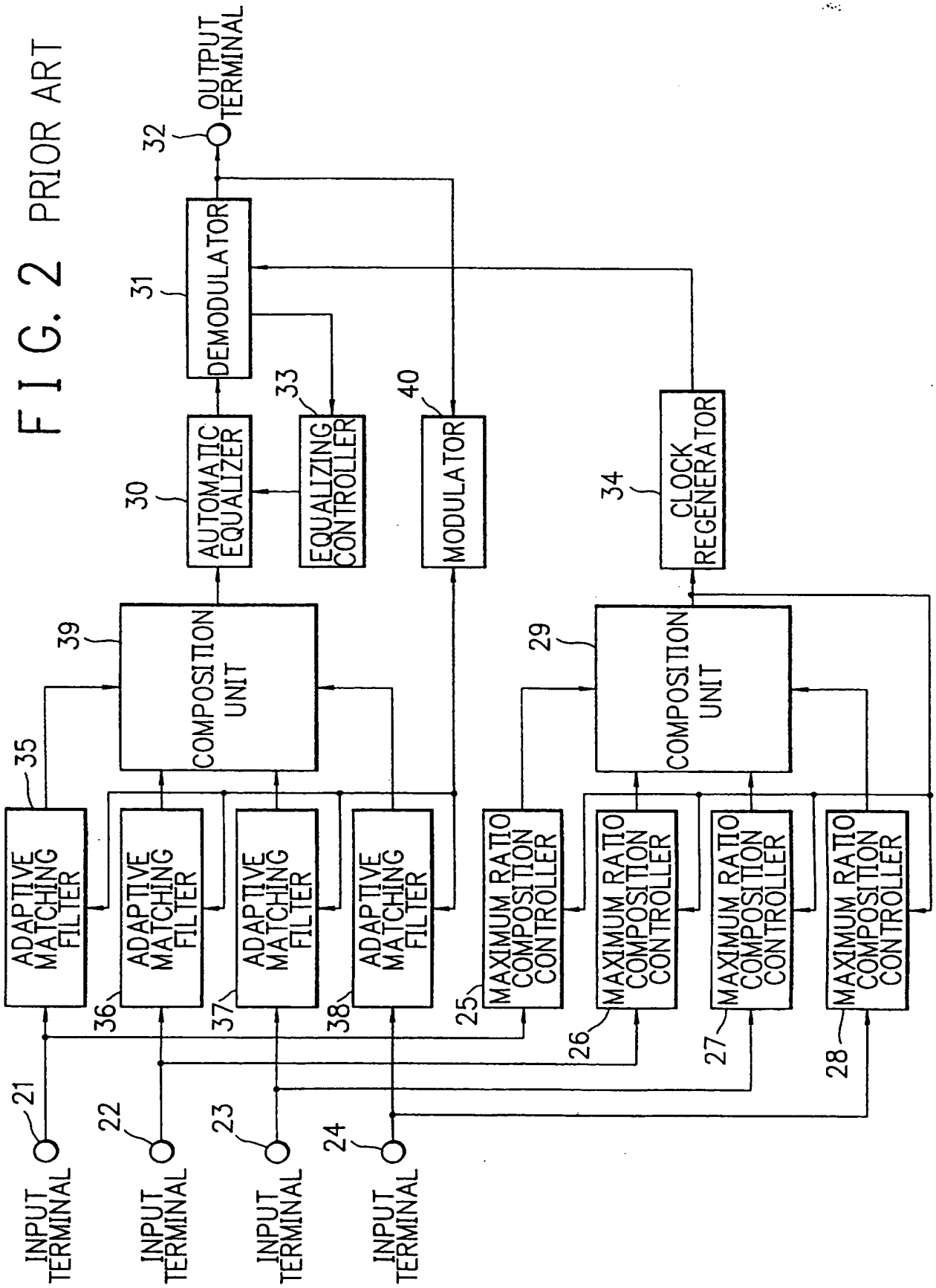


FIG. 3

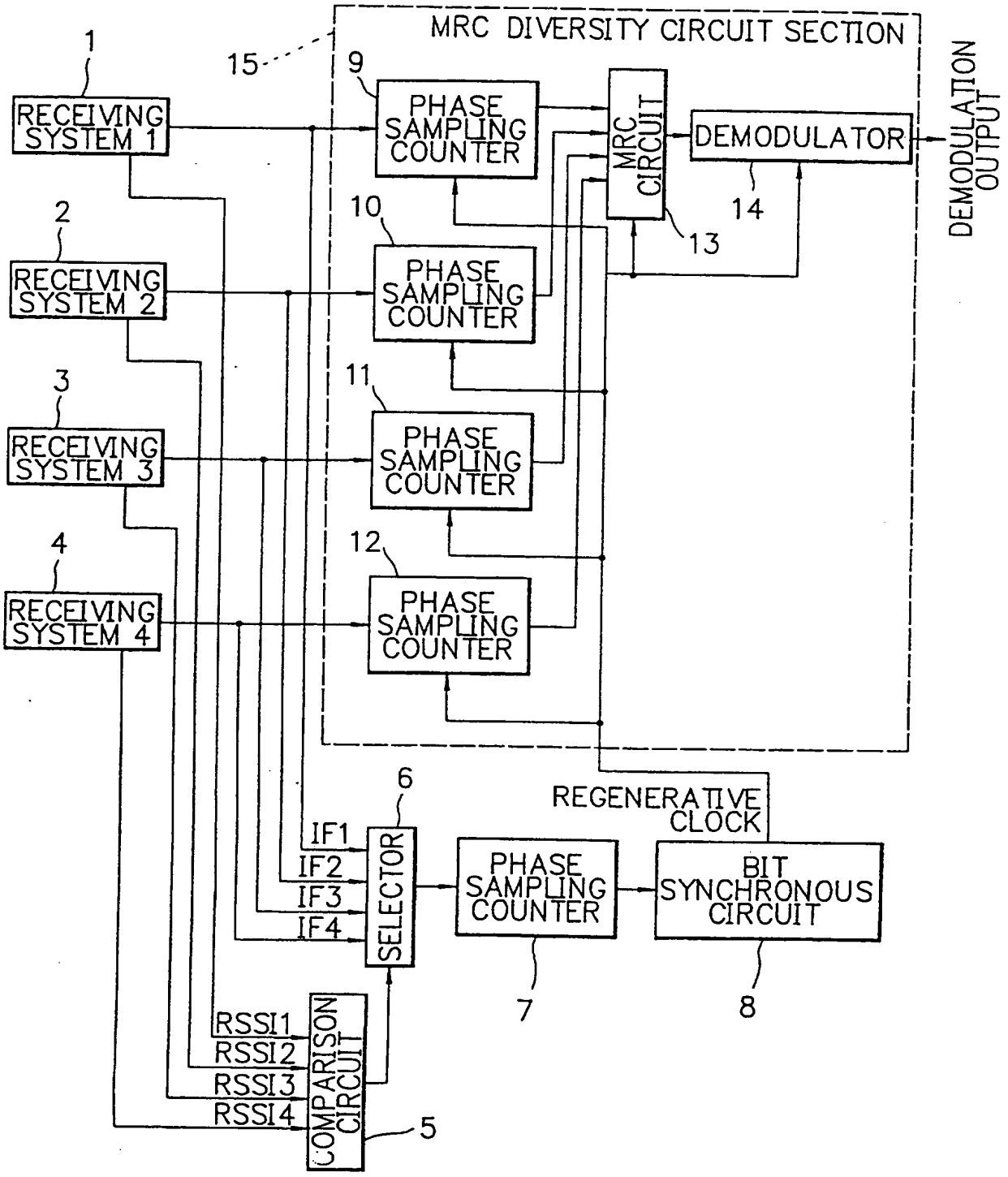

MRC DIVERSITY CIRCUIT SECTION
15
1
RECEIVING SYSTEM 1
2
RECEIVING SYSTEM 2
3
RECEIVING SYSTEM 3
4
RECEIVING SYSTEM 4
9
PHASE SAMPLING COUNTER
10
PHASE SAMPLING COUNTER
11
PHASE SAMPLING COUNTER
12
PHASE SAMPLING COUNTER
MRC CIRCUIT
13
DEMODULATOR
14
DEMODULATION OUTPUT
REGENERATIVE CLOCK
6
IF1
IF2
IF3
IF4
SELECTOR
PHASE SAMPLING COUNTER
7
BIT SYNCHRONOUS CIRCUIT
8
RSSI1
RSSI2
RSSI3
RSSI4
COMPARISON CIRCUIT
5

FIG. 4

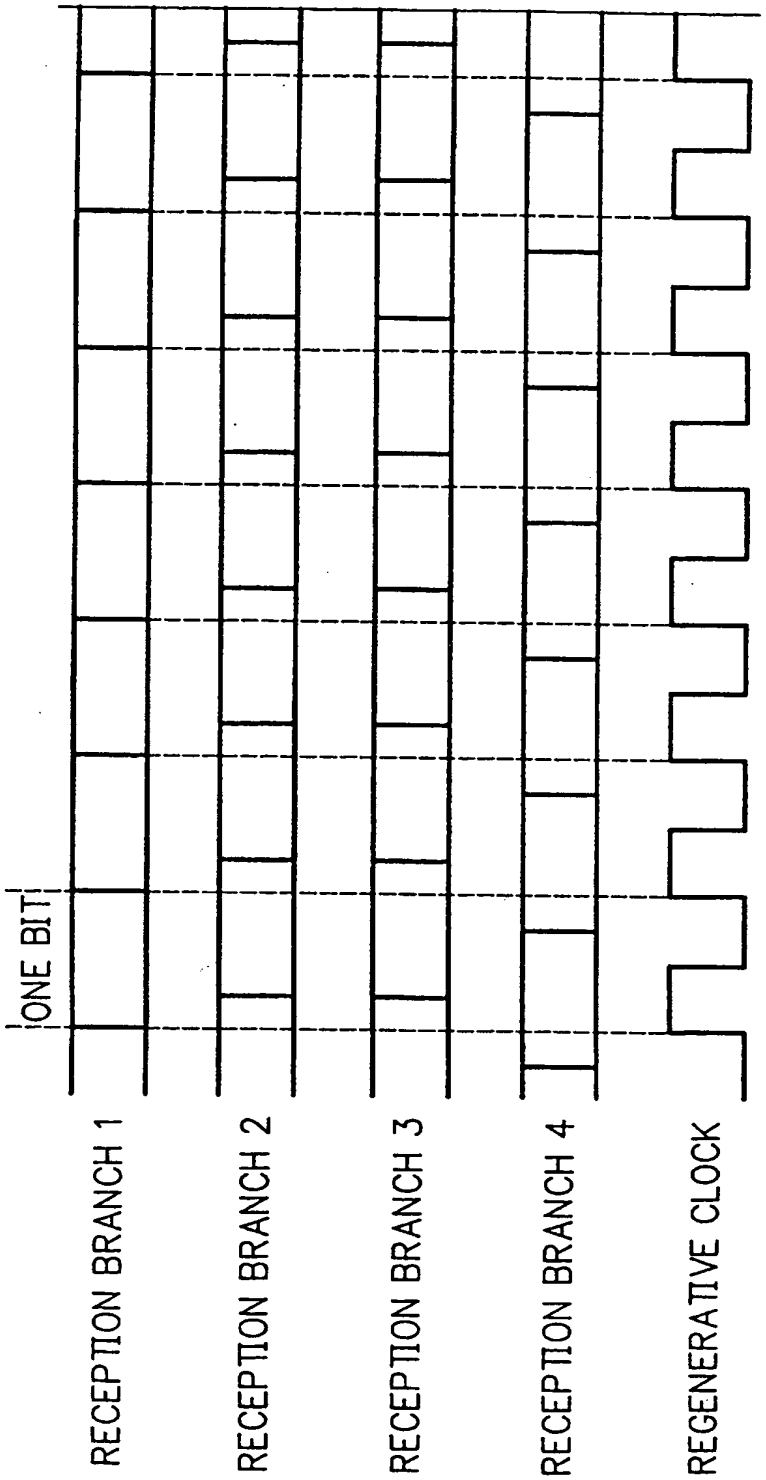
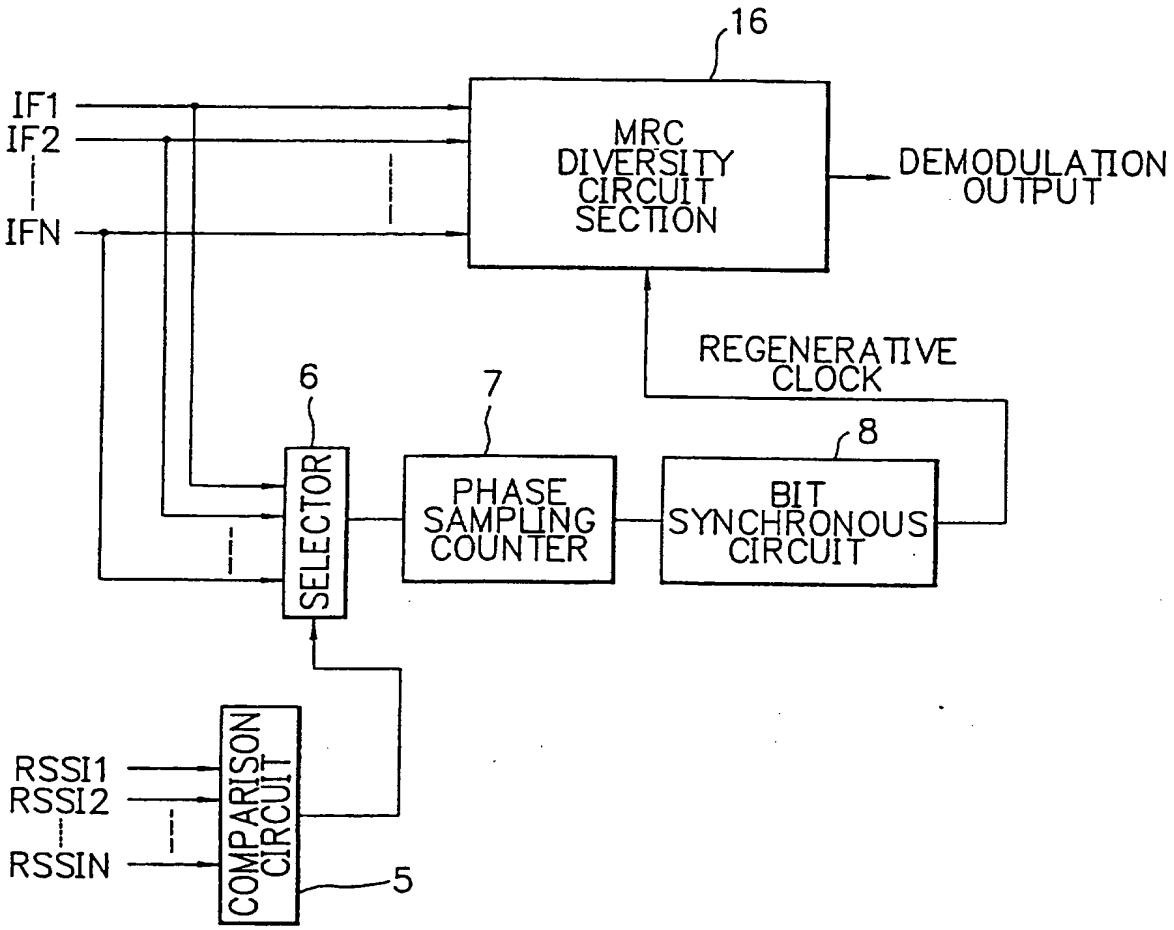

ONE BIT
RECEPTION BRANCH 1
RECEPTION BRANCH 2
RECEPTION BRANCH 3
RECEPTION BRANCH 4
REGENERATIVE CLOCK

FIG. 5


16
IF1
IF2
IFN
MRC DIVERSITY CIRCUIT SECTION
DEMODULATION OUTPUT
REGENERATIVE CLOCK
6
7
8
SELECTOR
PHASE SAMPLING COUNTER
BIT SYNCHRONOUS CIRCUIT
RSSI1
RSSI2
RSSIN
COMPARISON CIRCUIT
5

DELAYED DETECTION MRC DIVERSITY CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates to a delayed detection maximum ratio composition (hereinafter referred to as MRC) diversity circuit, for example for use in a mobile radio base station.

Description of the Prior Art

There exist various kinds of MRC diversity circuits. The conventional circuit of this kind is shown in Fig. 1 (hereinafter referred to as the first prior art).

The MRC diversity circuit of Fig. 1 employs maximum ratio composition controllers 25 to 28 as controllers for controlling diversity signals received at input terminals 21 to 24. A composition circuit 29 receives signals from the MRC controllers 25 to 28, and provides an output to an automatic equalizer 30 for removing inter-symbol interference caused by multipath distortion, the output of which is demodulated by a demodulator 31 to provide a base-band output signal at a terminal 32. An output from demodulator 31 is applied to an equalizing controller 33 to control the automatic equalizer. The output of the composition unit 29 is applied to a clock regenerator 34 to provide a clock signal for the demodulator 31. As is seen, the controllers 25 to 28 have no compensation function in terms of the time-base direction. Multipath differences of the received diversity signal can be large. There is thus the problem that when the time-base diffusion or distortion of the signals is increased, effective control can not be implemented.

Fig. 2 is a block diagram showing another known MRC diversity circuit (hereinafter referred to as the second

prior art) disclosed in Japanese Laid-Open Patent Application HEI 4-150320. In Fig. 2, reference numerals 35 to 38 represent adaptive matching filters, reference numeral 39 represents a composition unit, and reference numeral 40 represents a modulator.

A signal received by an antenna (not illustrated) is subjected to frequency conversion before being converted into an intermediate frequency signal, this being applied to input terminals 21 to 24 in every diversity. At this point, each signal is divided into two signal branches. One of the two signals is inputted to the adaptive matching filters 35 to 38 which have the constitution of transversal filters, and are subjected to the required signal processing, before being composed or combined into a single output signal by the composition unit 39. Inter-symbol interference caused by the multipath distortion is removed by the automatic equalizer 30, before being demodulated by the demodulator 31, and being outputted from the output terminal 32 as a base-band signal. On the other hand, a separate clock regeneration circuit is composed of maximum ratio composition controllers 25 to 28, composition unit 29, and clock regenerator 34.

The adaptive matching filters 35 to 38 are constructed as transversal filters, thus correlating the diffused signals with a reference signal from a modulator 40 connected to the output of the demodulator 31 at the taps of the transversal filter. The adaptive matching filters 35 to 38 behave such that they pick up the signal from the correlated taps, and time-base correction can thus be performed using the adaptive matching filters 35 to 38.

In the above described conventional MRC diversity circuit of the first prior art (Fig. 1), there is the

problem that the MRC diversity circuit has no time-base compensation function, and thus multipath differences become large so that the time-base distortion of the signal is increased, thereby resulting in the impossibility of effective control.

Also, there is the problem in the second prior art (Fig. 2) that although the time-base correction is implemented using the adaptive matching filters in the form of transversal filters, the circuit construction becomes complicated and expensive.

More generally in MRC diversity receivers all of the reception branches are demodulated. It then becomes a problem how to adjust bit synchronization. When all of the reception branches are provided with respective base-band circuits, such as synchronization circuits and so forth, the circuit becomes a large-scale one, and the interface between the base-band circuits of each of the systems becomes complicated.

Furthermore, as described in the invention of the Japanese Laid-Open Patent Application No. HEI 4-207821, when a sub received signal is composed with the main received signal such that the phase of the sub received signal corresponds with the phase of the main received signal with the signals adjusted to each other, there are problems that when the received field strength (hereinafter referred to as RSSI) of the main received signal deteriorates, achieving synchronization becomes difficult.

SUMMARY OF THE INVENTION

The present invention in its various aspects is defined in the independent claims below, to which reference should now be made. Advantageous features are set forth in the dependant claims.

As will be seen from the description below, a delayed detection MRC diversity circuit embodying the invention can adjust the timing of the reception branch with maximum RSSI so as to provide bit synchronization. Even if the RSSI of the reception branch which is adjusted for bit synchronization is weakened by fading or the like, it is still possible to adjust the bit synchronization properly.

Only a single MRC diversity circuit section is connected to all of the reception branches. Consequently, the greater part of the base-band circuit, such as the synchronization circuit and so forth, needs to be provided in only one circuit for the reception branch with maximum RSSI. A delayed detection MRC diversity circuit with proper reception characteristic can be realized without enlarging the size of the circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in more detail, by way of example, with reference to the drawings, in which:

Fig. 1 (described above) is a block diagram showing an example of this kind of conventional MRC diversity circuit;

Fig. 2 (described above) is a block diagram showing another example of a known kind of MRC diversity circuit;

Fig. 3 is a block diagram illustrating a first delayed detection MRC diversity circuit embodying the present invention;

Fig. 4 is a timing chart showing bit-synchronization timing between respective reception branches 1 to 4 and regenerative clock in the circuit of Fig. 3; and

Fig. 5 is a block diagram illustrating a second delayed detection MRC diversity circuit embodying the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will now be described in detail referring to the accompanying drawings.

Fig. 3 is a block diagram illustrating a first delayed detection MRC diversity circuit embodying the present invention. In Fig. 3, reference numerals 1 to 4 each represent respective reception branches. Diversity reception with four reception branches is illustrated in this embodiment. Reference numeral 5 represents a comparison circuit for selecting the reception branch with maximum RSSI in every symbol, by continuously comparing the RSSI of the respective reception branches. Reference numeral 6 represents a selector for selecting and outputting only the intermediate frequency (IF) signal from the reception branch which is selected by the comparison circuit 5. Reference numeral 7 represents a synchronization phase-sampling counter for phase sampling the intermediate frequency (IF) signal outputted from the selector 6. Reference numeral 8 represents a bit-synchronization circuit for generating clock pulses while adjusting the bit timing to be synchronous with the output from the synchronization phase-sampling counter 7.

Furthermore, reference numeral 15 represents an MRC diversity circuit section. The MRC diversity circuit section 15 of this embodiment comprises synchronous phase-sampling counters 9 to 12 for phase sampling the intermediate frequency signals from the reception branches 1 to 4 respectively, a composition circuit 13 for composing the phase values from the phase-sampling counters 9 to 12 respectively, and a demodulation circuit 14 for demodulating on the basis of the composed phase value. The regenerated clock from the bit synchronization circuit 8 is inputted to each of the phase-sampling counters 9 to 12, to the composition circuit 13, and to the demodulation circuit 14, and thus the MRC diversity section 15 operates using the clock as a reference.

The operation thereof will now be described. Fig. 4 is a timing chart showing the bit synchronization timing between the respective reception branches 1 to 4 and the regenerated clock. The comparison circuit 5 continuously compares the RSSI from the respective reception branches 1 to 4 with one another in every symbol period, and outputs the information to the selector 6 while continuously detecting the reception branch with the maximum RSSI. In Fig. 4, the reception branch 1 with maximum RSSI is selected for synchronization.

The selector 6 selects only the intermediate frequency signal from the reception branch which has the maximum RSSI, on the basis of the information from the comparison circuit 5, to input to the phase-sampling counter 7, before adjusting the bit timing of the intermediate frequency signal at the bit-synchronization circuit 8 to output the regenerated clock, before inputting the outputted regenerated clock to the MRC diversity circuit section 15. The MRC diversity circuit

section 15 implements phase sampling of the intermediate frequency signals from the respective reception branches 1 to 4, an MRC operation, and a demodulating operation using the timing of the regenerated clock.

Consequently, it is not necessary to adjust synchronization independently in every reception branch. The circuit is capable of composing the intermediate frequency signal into the phase difference information with maximum RSSI and more positive bit timing. A delayed detection MRC diversity circuit with superior receiving characteristics is obtained.

Fig. 5 is a block diagram illustrating another delayed detection MRC diversity circuit embodying the present invention. An MRC diversity circuit section 16 comprises N radixes of diversities, counters, a composition unit and so forth. The MRC diversity circuit section 16 is different from the MRC diversity circuit section 15 which is shown in Fig. 3. Namely, the delayed detection MRC diversity circuit of Fig. 5 is capable of implementing not only four diversities as shown in Fig. 3 but rather any number of diversities.

The MRC diversity circuit section is capable of operating in relation to any circuit which performs this kind of composing operation and demodulating operation with required timing, which does not employ a phase-sampling counter.

As described above, the delayed detection MRC diversity circuit has the constitution that it causes bit synchronization to adjust the reception branch with the maximum RSSI. The intermediate frequency signal from all of the reception branches can be converted into phase difference information with more positive bit timing to be composed. As a result, a circuit with better reception

characteristics such as fading characteristics and high reliability can be realized.

Furthermore, only a single MRC diversity circuit section is connected to all of the reception branches. Consequently, the greater part of the base-band circuitry, such as the synchronization circuit and so forth, can do with only one circuit for the reception branch with maximum received signal strength even if any number of diversities exist. Thus a simple and inexpensive circuit is capable of being realized.

While preferred embodiments of the invention have been described using specific terms, such description is for illustrative purpose only, and it is to be understood that changes and variations may be made without departing from the scope of the following claims.

CLAIMS:

1. A delayed detection MRC diversity circuit which composes a signal received by a plurality of reception branches with required bit-synchronous timing for demodulation, and comprising:

means for detecting the reception branch with maximum RSSI (receiving field strength);

means for regenerating clock signals by bit synchronizing the signal received by the reception branch with maximum RSSI; and

means for composing and demodulating the signals received by the plurality of reception branches with timing synchronization from the clock signals.

2. A delayed detection MRC diversity circuit according to claim 1, wherein the means for detecting the reception branch with maximum RSSI compares the RSSI in every symbol received by the plurality of reception branches.

3. A delayed detection MRC diversity circuit comprising:

means for continuously detecting the reception branch with maximum RSSI;

means for regenerating clock signals by synchronizing the signal received by the reception branch with maximum RSSI; and

means for composing and demodulating the signals received by the plurality of reception branches with timing synchronization from the clock signals, to ensure bit synchronization without further synchronization operation.

4. A method of delayed detection MRC diversity reception which composes a signal received by a plurality of reception branches with required bit synchronous timing for demodulation, the method comprising the steps of:

detecting a reception branch with maximum RSSI;

regenerating clock signals by bit synchronizing the signal received by the reception branch with maximum RSSI; and

composing and demodulating the signals received by the plurality of reception branches with timing synchronization from the clock signals.

5. A method of delayed detection MRC diversity reception according to claim 4, wherein the step of detecting the reception branch with maximum RSSI comprises comparing the RSSI in every symbol which is received by the plurality of reception branches.

6. A method of delayed detection MRC diversity reception, comprising the steps of:

continuously detecting the reception branch with maximum RSSI;

regenerating clock signals by synchronizing the signal received by the reception branch with maximum RSSI; and

composing and demodulating the signals received by the plurality of reception branches with timing synchronization from the clock signals, to ensure bit synchronization is ensured without a further synchronization operation.

7. A delayed detection MRC diversity circuit, substantially as herein described with reference to Fig. 3 et seq of the drawings.

8. A method of delayed detection MRC reception, substantially as herein described with reference to Fig. 3 et seq of the drawings.

The Patent Office

12

Application No:	GB 9712960.5	**Examiner:**	B.J.SPEAR
Claims searched:	1-8	**Date of search:**	25 September 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H4L (LDDRS); H4P (PSB, PSEX, PSX, PEM)

Int Cl (Ed.6): H04B 7/02, 7/08, 7/12; HO4L 1/20

Other: Online: WPI, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
	NONE	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.